February 19, 2002

INFORMATION DISCLOSURE STATEMENT letter

To Whom It May Concern:

The following documents are included in form PTO/SB/08A Information Disclosure Statement by Applicant as a bibliography for the application having the following title and applicant.

Title: Shared Parallel Digital-to-Analog Conversion

Applicant: Charles D. Murphy

Here, the documents are discussed as they relate to the specification and claims of the application.

The present invention proposes a machine for digital-to-analog (D/A) conversion in which a digital number value to be converted to an analog value is compared to a reference digital signal such as a digital count. One or both of the digital values change as a function of time while an analog reference signal also changes as a function of time. When the digital values are detected as being equal by a digital comparator, the value of the analog reference signal is recorded as the desired analog value. Important embodiments of the invention are aimed at shared parallel D/A conversion. For instance, a time-varying digital count can be shared by a multiplicity of simultaneous conversion operations. Also, a time-varying reference signal can be shared by a multiplicity of simultaneous conversion operations, with different analog outputs recorded using sample-and-hold circuits triggered at different times.

"The Art of Electronics" by Paul Horowitz and Winfield Hill is a comprehensive textbook on basic design techniques for analog and digital circuits. Pages 614 to 620 of the second edition discuss digital-to-analog (D/A) converters, while pages 621 to 641 discuss analog-to-digital (A/D) converters. Several of the various types of D/A converters are discussed in the specification of the present invention, as well as some of the A/D converters. The A/D converters are relevant because some of the embodiments of the invention are similar in operation to certain A/D conversion techniques. Also, some of the A/D converters, such as successive-approximation converters and half-flash converters, have as elements internal D/A converters.

Several US patents provide examples of prior art relevant to the present invention.

US Patent 6,346,901 entitled "Digital-to-analog conversion circuit" and issued to M. Aiura, Y. Nakatani, and T. Kumazaki on February 12, 2002 discusses a D/A converter using switched current sources.

US Patent 6,297,759 entitled "Digital-to-analog converter with high-speed output" issued to L.L. Lewyn on October 2, 2001 discusses a D/A converter which uses "at least one resistive converter (RDAC) segment" in each claim. The main purpose of the invention of US Patent 6,297,759 is to eliminate "glitch disturbances" in D/A converters, such as output voltage spikes, that require time to settle and disappear.

US Patent 6,172,634 entitled "Methods and apparatus for providing analog-fir-based line-driver with pre-equalization" issued to R.H. Leonowich, O. Shoaei, and A. Shoval on January 9, 2001 describes a current-steered or current-switched D/A converter.

US Patent 6,169,509 entitled "Switched capacitor type D/A converter and display driver" issued to K. Abe on January 2, 2001 describes a switched capacitor D/A converter. The converter is similar to prior art D/A converters excepting fast reset, offset cancellation, and incorporation into a display driver. While the specification states that "All switched capacitor type D/A converters in the liquid crystal driver can share one external drive voltage source", there is no sharing of internal circuit elements.

US Patent 6,157,334 entitled "Digital-analog converter, circuit board, electronic device and liquid crystal display device" and issued to M. Kimura on December 5, 2000 describes a D/A converter based on resistive ladder techniques.

US Patent 6,052,074 entitled "Multi-channel digital-to-analog converters comprising with a plurality of converter units" issued to J. Iida on April 18, 2000 describes parallel current-switched D/A converters, particularly intended as drivers for tri-color display elements. Transistors corresponding to similar current levels in different converters are fabricated in close physical proximity to one another so that they have approximately the same parasitic resistances. The circuit elements of the D/A converters are thus interleaved. However, the invention includes a single input and a single output corresponding to each D/A converter for several embodiments. Shared switching circuitry separate from the converters themselves can be used to select a D/A converter output to be placed on a shared bus line.

Some embodiments of the invention of US Patent 6,052,074 "share one common input transistor". The purpose of this is to eliminate variations resulting from having multiple, different input transistors. However, the "input transistor" in question are in fact part of a reference signal circuit for a set of current mirrors. Each D/A converter has a separate set of transistors that produce scaled currents driven by a reference current source and the "input transistor". The current mirrors for the converters can share the reference. Such sharing is not a new idea in the context of current mirror design. In the context of D/A conversion and the present invention, the shared element is not one that changes, and using it does not result in large savings of resources.

US Patent 5,808,576 entitled "Resistor string digital-to-analog converter" and issued to J. Chloupek, H.T.H. Yung, and S.W. Yang on September 15, 1998 describes a D/A converter based on an array of resistors in a string and means for selectively switching resistors into or out of a conversion circuit.

US Patent 5,764,173 entitled "Digital to analogue converter having input control bits for selecting a pulse width modulated output signal" issued to D.W. Flynn on June 9, 1998 discusses a D/A converter with switched output stages applied to a summing junction for producing an analog output. The invention includes an embodiment with a pulse-width modulated output signal.

US Patent 5,748,128 entitled "Reduced current quadratic digital/analog converter with improved settling time" issued to M. Bruccoleri, M. Demicheli, G. Patti, and V. Pisati on May 5, 1998 discusses a D/A converter based on an R-2R resistor network. The invention comprises a cascade of linear D/A converter stages.

US Patent 5,703,586 entitled "Digital-to-analog converter having programmable transfer function errors and method of programming same" issued to H.J. Tucholski on December 30, 1997 describes a D/A converter in which a "Main Converter" and one or more "Sub-Converters" provide analog signals that are added to produce the D/A converter output. The purpose of the Sub-Converters is to compensate for errors in the Main Converter based on error estimates derived from a Calibration Sequence.

US Patent 5,703,582 entitled "DAC with feedback control for current source bias during non-display period" and issued to S. Koyama, T. Nozawa, A. Terukina, and Y. Suzuki on December 30, 1997 describes a switched-current D/A converter with feedback compensation of converter errors during periods when the D/A converter output is not needed. The invention is particularly designed for driving display devices.

US Patent 5,663,728 entitled "Digital-to-analog converted (DAC) and method that set waveform rise and fall times to produce an analog waveform that approximates a piecewise linear waveform to reduce spectral distortion" and issued to K.A. Essenwanger on September 2, 1997 discusses a D/A converter which produces a waveform that is composed of linear transitions between the analog values corresponding to valid code words. This is in lieu of prior art D/A converters which implement a zero-order hold resulting in a staircase output signal.

US Patent 5,600,321 entitled "High speed, low power CMOS D/A converter for wave synthesis in network" issued to J.M. Wincn on February 4, 1997 discusses a current-switched D/A converter.

US Patent 5,594,438 entitled "Analog-to-digital converter" issued to S. Panaoussis on January 14, 1997 discusses a circuit that can function as either a D/A converter or an A/D converter. The circuit for D/A conversion involves bit-wise generation of a series of analog signals which are passed through a sequence of stages. Each stage modifies the input analog signal according to bit values. The analog signal after the last stage is the desired analog output.

US Patent 5,539,405 entitled "DAC achieving monotonicity with equal sources and shift array therefore" issued to J.P. Norsworthy on July 23, 1996 discusses a current switched D/A converter which uses differential techniques to modify its output from one use to the next. Given a first input and a corresponding first output, the next input is used to switch on or off the current sources without first resetting them all to an initial value. The goal is to have the output corresponding to the first input shift smoothly to the output corresponding to the next input. This technique is effective when successive inputs are highly correlated. When they are uncorrelated, or independent, there is no benefit to preserving the states of the current sources from one input to the next.

US Patent 5,515,047 entitled "Converter, offset adjustor, and portable communication terminal unit" and issued to K. Yamakido, Y. Kobayashi, M. Otsuka, T. Okazaki, Y. Ishihara, N. Nishikawa, and Y. Tamba on May 7, 1996 discusses a current-switched D/A converter. The invention uses a standard cell "unit D/A converter" with "current attenuators or current amplifiers" to implement conversion of digital representation elements with differing analog amplitude values.

US Patent 5,508,702 entitled "BiCMOS digital-to-analog conversion" and issued to J.R. Estrada and R.A. Mentzer on April 16, 1996 describes a switched-current D/A converter in which the various current mirror transistors of the converter output are biased from a common reference transistor, similarly to that of the invention of US Patent 6,052,074.

US Patent 5,446,457 entitled "Current-summing digital-to-analog converter with binarily weighted current sources" and issued to M.H. Ryat on August 29, 1995 describes a resistor-ladder or R-2R D/A converter.

US Patent 5,307,065 entitled "Digital-to-analog converter" and issued to N. Tokuhiro on April 26, 1994 describes a resistor-ladder D/A converter.

US Patent 5,283,579 entitled "Digital to analog converter having high multiplying bandwidth" and issued to A. Tasdighi, R.A. Levinson, Q.V. Huynh, and J.M. Caruso on February 1, 1994 describes a resistor-ladder D/A converter with selection from among several reference voltages. Some input bits are used to select a reference voltage applied to the resistors, while the other input bits are used to selectively connect the resistors.

US Patent 5,227,783 entitled "Telemetry apparatus and method with digital to analog converter internally integrated within C.P.U." and issued to H.L. Shaw, R.B. Smith, L.E. Cunningham, B.E. Rishel, J.P. Gioannini, and W.B. Harkey on July 13, 1993 discusses a 16-channel D/A converter which appears in figure 39 of the patent along with elaborations of D/A converter elements in figures 40 through 53.

With respect to the claims of US Patent 5,227,783, the patent covers particular details of a system for processing telemetry data, including various embodiments for storing data, encoding data, and displaying data. With respect to D/A conversion and the present invention, the 16-channel D/A converter of US Patent 5,227,783 has a global processing element and 16 local processing elements 3906 which are D/A converter (DAC) loaders. However, as clearly shown in the figure, D/A conversion is actually implemented in a set of parallel DACs 3912 which do not have any shared circuit elements but which may have a common voltage reference 3914.

US Patent 5,162,801 entitled "Low noise switched capacitor digital-to-analog converter" and issued to S.R. Powell and A.G. Mellissinos on November 10, 1992 describes a switched-capacitor D/A converter.

US Patent 5,148,164 entitled "Current generating device for complementarily generating two currents of different magnitudes in response to one-bit data" and issued to Y. Nakamura and T. Kumamoto on September 15, 1992 describes a D/A converter in which two analog currents are generated for one digital input. In an embodiment of the invention, a digital video signal applied in parallel is converted to a serial sequence of digital numbers for conversion to analog values.

US Patent 5,091,728 entitled "D/A and A/D converters utilizing weighted impedances" and issued to C.C. Chang on February 25, 1992 discusses a resistor-ladder D/A converter. In an embodiment of the invention, the D/A converter can be used as part of an A/D converter. The D/A converter can also be used to produce an analog signal which is the sum of several analog signals corresponding to several digital numbers, without first adding the digital numbers.

US Patent 5,057,838 entitled "D/A converter having centered switching sequence and centered arrangement of converter segment groups" and issued to K. Tsuji, T. Iida, and T. Satoh on October 15, 1991 describes a technique for implementing several D/A converters on the same chip substrate. The D/A converters do no share circuit elements even though they may operate in parallel. The main aim of the patent is to interleave elements of the various converters so that they all have approximately the same electrical characteristics.

US Patent 4,982,192 entitled "Digital-to-analog converter having common adjustment means" and issued to F. Murooka on January 1, 1991 describes D/A converters implemented in parallel on the same chip. However, the main goal of the parallel implementation is to enable a common power source and a common bias circuit.

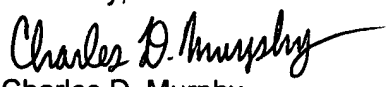
US Patent 4,872,011 entitled "Plural stage switched capacitor integrating digital-to-analog converter" and issued to M.J.M. Pelgrom and A.C.J. Duinmaijer on October 3, 1989 describes a D/A converter in which an analog output is generated by selectively switching to implement an integration function.

US Patent 4,484,178 entitled "Digital-to-analog converter" and issued to J.L. Lovgren, G.C. Thomas, and J.T. Trnka on November 20, 1984 describes a pulse-width modulation D/A converter.

I, the inventor of the present invention have been unable to find any prior art closely similar to the material of the present invention. To the best of my knowledge, the ideas of digital single-slope integration D/A conversion and parallel D/A converters with simultaneously shared circuit elements having time-varying properties are new and deserving of patent protection.

This concludes this INFORMATION DISCLOSURE STATEMENT letter.

Sincerely,



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